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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF: :

SHIGENOBU MAEDA : EXAMINER: PYONIN, A.

SERIAL NO: 09/761,738

FILED: JANUARY 18, 2001 : GROUP ART UNIT: 2824

FOR: MANUFACTURING METHOD OF SEMICONDUCTOR WAFER, . . .

APPEAL BRIEF UNDER 37 C.F.R. §1.192

10 # Appeal Brief 7/26/02 DBun

ASSISTANT COMMISSIONER OF PATENTS
WASHINGTON, DC 20231

SIR:

This is an appeal from a final Office Action mailed February 21, 2002. A Notice of Appeal was timely filed on May 21, 2002.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is **MITSUBISHI DENKI KABUSHIKI KAISHA** having address at 2-3, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100-8310 JAPAN.

II. RELATED APPEALS AND INTERFERENCES

Appellants, Appellants' legal representative and the assignees are aware of no appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF THE CLAIMS

Claims 21-24 stand finally rejected and are herein appealed.

IV. STATUS OF THE AMENDMENTS

An amendment was timely filed on January 24, 2002, and a Supplemental Amendment was filed on February 12, 2002 to correct a grammatical error in the claims. In a Final Office Action mailed February 21, 2002, the Examiner finally rejected Claims 21-24. A Notice of Appeal was timely filed on May 21, 2001. The attached Appendix I reflects Claims 21-24 as presently pending on appeal.

V. SUMMARY OF THE INVENTION

The invention is directed to a method of manufacturing a semiconductor device. As described in the specification, the field of semiconductor device manufacturing has experienced a recent trend in that circuit components or elements called "intellectual properties" are being combined into highly integrated circuits.[1] Each of the intellectual properties is itself a large scale integrated circuit composed of many circuit elements combined to provide an overall function for the intellectual property.[2] However, conventional semiconductor device manufacturing techniques are inflexible and allow the mass production of relatively few kinds of highly integrated circuits, making profits difficult to realize in the integrated circuit manufacturing industry.[3] The present invention is directed to a flexible

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[1]Specification at page 2, line 22-page 3, line 2.

[2]Id.

[3]Specification at page 3, lines 3-10.

system for manufacturing semiconductor devices that allows the mass production of several kinds of highly integrated circuits.[4]

Figure 35 of the present specification is a circuit diagram showing a plurality of intellectual properties (IP1 through IP4) of a personal computer integrated into a single semiconductor chip.[5] Figure 38 is a block diagram of an exemplary semiconductor manufacturing apparatus in accordance with the claimed invention. As seen in Figure 38, the manufacturing apparatus includes a mask pattern generating portion 126 for generating a mask pattern for each intellectual property of the entire circuit of the personal computer, and a mask pattern transfer portion 127 for transferring the mask patterns to a predetermined portion of a semiconductor chip based on a layout pattern provided by the synthesizing portion 118.[6] As seen in Figure 39, each mask pattern is provided with superposition marks 132 used for arranging mask patterns on the semiconductor chip. The mask patterns of the plural intellectual properties are arranged side by side by overlapping the superposition marks of adjacent intellectual properties as shown in Figure 40.

VI. ISSUES

The first issue for review is whether one or more of Claims 21-24 are unpatentable as being indefinite under 35 U.S.C. §112, second paragraph? The second issue for review is whether one or more of Claims 21-24 are unpatentable under 35 U.S.C. §102 as being anticipated by U.S. Patent No. 3,760,384 to Krolikowski et al.?

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[4]Specification at page 9, lines 11-12.

[5]Specification at page 31, lines 7-10.

[6]Specification at page 34, lines 16-23.

VII. GROUPING OF THE CLAIMS

For the first and second issues, Claims 21-24 stand or fall together.

VIII. ARGUMENT

A. THE FIRST ISSUE

The term "intellectual properties" in Claims 21 and 22 is not indefinite under 35 U.S.C. §112, second paragraph.

A claim is not indefinite under 35 U.S.C. § 112, second paragraph, if the scope of the claim would be reasonable ascertainable by those skilled in the art. *Ex parte Porter*, 25 USPQ2d 1144, 1145 (Bd. Pat. App. & Inter. 1992). Appellants first note that the term "intellectual property" has an accepted meaning in the semiconductor industry. Specifically, intellectual properties are predefined circuits that can be formed on a semiconductor wafer as a component of a larger operational circuit. Attached in Appendix II are internet web page print-outs that use the term intellectual property in this context. Thus, "intellectual property" as recited in Appellants claims 21 and 22 is not indefinite to one of ordinary skill in the art of semiconductor devices.

Moreover, under 35 U.S.C. § 112, second paragraph, the specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention. When the specification states the meaning that a term in the claim is intended to have, the claim is examined using that meaning, in order to achieve a complete exploration of the applicant's invention and its relation to the prior art. *In re Zletz*, 893 F.2d 319, 13 USPQ2d 1320 (Fed. Cir. 1989). Appellants submit that in addition to its accepted meaning in the art, the term "intellectual properties" is defined in the

specification with sufficient clarity to enable one of ordinary skill in the art to reasonably ascertain the scope of the claim.

Specifically, the specification reads as follows:

> This is followed by a move afoot to form a highly integrated circuit by combining various circuit components (referred to as "microcells" or "IP (Intellectual Property)"), each composed of circuit elements and performing a certain function.[7]

Moreover, as noted in the Summary of the Invention section above, Figures 35-40 and the accompanying text describe the intellectual properties as functional circuits such as the microprocessor IP1, memory controller IP2, cache memory IP3, memory IP4, and graphics controller IP5 shown in Figure 35. One of ordinary skill in the art would be able to ascertain from this specific disclosure and the disclosure as a whole that the intellectual properties are circuits that include a plurality of circuit elements to perform a certain function.

Finally, contrary to the position in the Final Action, the definition of intellectual properties in the specification is not repugnant to the accepted meaning of this term. First, as is evidenced from the above discussion, Appellants use of the phrase intellectual property is consistent with an industry accepted meaning for this term. Moreover, repugnance signifies an inconsistent meaning. However, one can easily understand how "intellectual property" may be used to describe a functional circuit because such circuits frequently embody "intangible creations of the human intellect that are protected by law," which is the accepted meaning of intellectual property, as the Final Action quotes.[8] Therefore, the rejection under 35 U.S.C. §112, second paragraph, should be reversed.

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[7]Specification at page 2, line 24 - page 3, line 2.

[8]Official Action at page 2, paragraph 3.

B. THE SECOND ISSUE

Krolikowski et al. does not teach arranging each mask pattern of the plurality of intellectual properties for a layout pattern as recited in Claim 21.

As noted in the argument of the first issue, intellectual properties are circuits that include a plurality of circuit elements to perform a certain function. Claim 1 recites arranging each mask pattern of the plurality of intellectual properties for a layout pattern. Thus, Claim 1 is directed to arranging mask patterns of a plurality of functional circuits that each include a plurality of circuit elements. As an example of this, the microprocessor IP1 in Figure 35 is an intellectual property that performs the function of processing using various circuit elements such as arithmatic logic units (ALU) and memory registers, for example. In contrast, the reference to Krolikowski et al. discloses a method of fabricating an FET memory chip. The method uses separate masks to define and form the different regions of the FET devices. These masks are mask patterns of portions of a discrete electronic component (i.e. the FET) and not mask patterns of a plurality of intellectual properties. Thus, Krolikowski et al. does not teach the limitation of arranging each mask pattern of the plurality of intellectual properties for a layout pattern. Therefore, Claim 21, and Claims 22-24 which depend therefrom, patentably define over Krolikowski et al.

IX. CONCLUSION

Appellants submit that Claims 21-24 meet the requirements of 35 U.S.C. §112, second paragraph, and that the prior art neither discloses nor suggests the method

of manufacturing a semiconductor device as recited in Claims 21-24. Accordingly, it is respectfully requested that all the rejections still pending in the final Office Action be REVERSED.

Respectfully submitted,

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APPENDIX I

CLAIMS ON APPEAL

21. (Amended) A method of manufacturing a semiconductor device for building a circuit composed of combined plural intellectual properties into a semiconductor chip, comprising:

arranging each mask pattern of said plural intellectual properties for a layout pattern.

22. (Twice Amended) The method of manufacturing a semiconductor device according to Claim 21, wherein

said each mask pattern of said plural intellectual properties has a mark for positioning, and

positioning of said mask patterns is performed by superposing one of said marks on another of said marks.

23. A semiconductor device manufactured by the method according to Claim 21.

24. A semiconductor device manufactured by the method according to Claim 22.

APPENDIX II

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  - IP Viewpoint
  - Press Releases
  - Success Stories
- Product Information
  - Bluetooth Platform
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COMMISSIONER FOR PATENTS
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RE: U.S. Application
Serial No: 09/761,738
Filed: January 18, 2001
Inventor: Shigenobu MAEDA
For: Manufacturing Method of Semiconductor . . .

SIR:

Attached hereto for filing are the following papers:

APPEAL BRIEF w/ APPENDICES I AND II (IN TRIPLICATE)

Our check in the amount of $ --320.00-- is attached covering any required fees. In the event that any variance exists between the amount enclosed and the Patent Office charges for filing the above-noted documents, including any fees required under 37 CFR 1.136 for any necessary Extension of Time to make the filing of the attached documents timely, please charge or credit our Deposit Account No. 15-0030. Further, if these papers are not considered timely filed, then a petition is hereby made under 37 C.F.R. 1.136 for the necessary extension of time. A duplicate copy of this sheet is attached.

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